Linear MAP Decoding of Convolutional Codes

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THE UNIVERSITY OF SYDNEY

Signal processing

> TRL 2-3

Executive statement

A novel Linear Maximum a Posteriori (LMAP) decoding method and decoder architecture for rate 1/2 convolutional codes that significantly reduces decoding complexity and delay while matching optimal MAP decoding performance.

Solution

The LMAP decoder introduces a dual encoder structure comprising forward and backward soft-input soft-output (SISO) decoding modules with shift registers, enabling bidirectional MAP decoding by combining forward and backward outputs. This approach represents the BCJR MAP decoding process through simple linear shift registers, allowing efficient hardware implementation and parallel processing. The method supports recursive systematic codes (RSC) and non-systematic codes (NSC) with reduced computational complexity and superior cache utilization. It achieves the same error-correction performance as BCJR decoding but with dramatically reduced decoding time, unlocking practical decoding of very large state convolutional codes.

Intellectual Property Status

Provisional application 2025900174

Key advantages

- Significantly reduced computational complexity compared to BCJR algorithm
- Substantially lower decoding delay with up to 331x speed improvement for large memory codes
- Simple architecture based on linear shift registers enabling efficient hardware and parallel software implementations
- Superior cache utilization due to localized register access
- Applicable to both recursive systematic codes (RSC) and non-systematic codes (NSC)
- Supports tail-biting convolutional codes with near-capacity performance
- Offline parameter determination enables real-time efficient decoding

Problems solved

- High computational complexity and memory access delays in conventional MAP decoding (BCJR)
- Difficulty decoding convolutional codes with large constraint lengths ($k \geq 10$) using existing algorithms
- Rate loss caused by tail bits in traditional decoding methods
- Trade-off between complexity and performance in list Viterbi decoders
- Inefficiency in decoding very large state convolutional codes (VLSC)

Market applications

- Cellular networks and 4G/5G communication systems
- Wi-Fi and wireless local area networks
- Satellite and space communications
- Data storage and magnetic recording devices
- Turbo code and serial concatenated code decoders
- Short blocklength communication systems requiring low latency and high reliability
- Hardware implementations in communication chipsets and FPGA/ASIC decoders

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